MN662750CDK

Signal Processing LSI for CD–ROM Drives

■ Overview

The MN662750CDK is a CD–ROM signal processing LSI that, on a single chip, combines optics servos for the CD player (focus, tracking, and traverse servos), digital signal processing (EFM demodulation and error correction), digital servo processing for the spindle motor, digital filter, and D/A converter, so thus covers all signal processing functions from the head's RF amplifier onward.

■ Features

- Optics servo
  - Focus, tracking, and traverse servos
  - Automatic adjustment functions for FO/TR gain, FO/TR offset, and FO/TR balance
  - Built-in D/A converter for drive voltage output
  - Built-in dropout countermeasures
  - Support for anti-shock functions
  - Built-in track cross counter
  - Lens vibration suppression function
- Digital signal processing
  - Built-in DSL and PLL
  - Frame synchronization detection, holding, and insertion
  - Subcode data processing

    Subcode Q data CRC check

    Built-in subcode Q data register
  - CIRC error detection and correction

    C1 decoder: duplex error correction

    C2 decoder: triplex error correction

    Includes 16-K bits of RAM for use in de-interleaving
  - Audio data interpolation

    Average interpolation or retention of previous values

    Soft muting

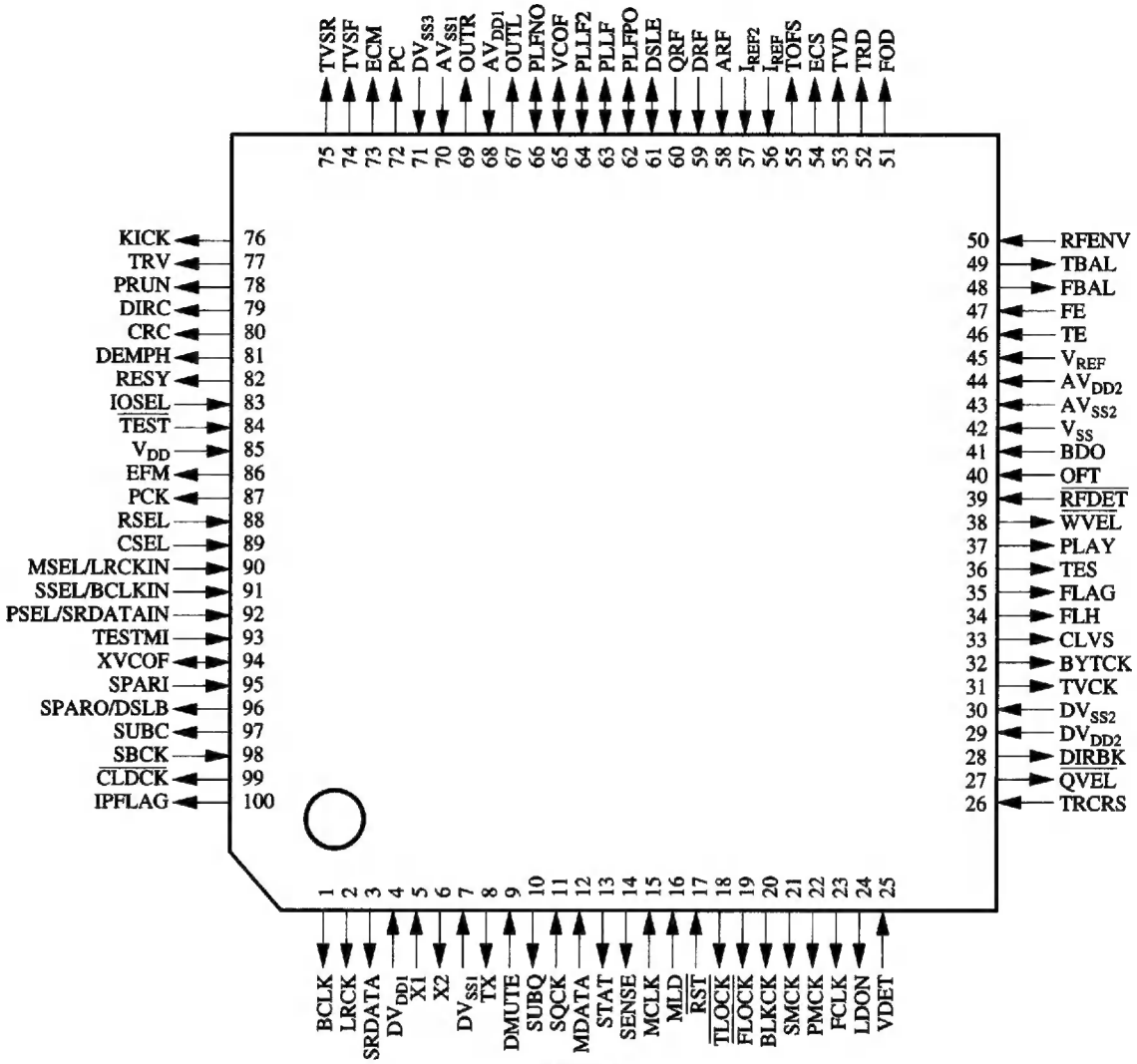
    Independent digital attenuation for left and right channels (256 levels)

    Monaural playback function
  - Software attenuation (256 levels)
  - Digital audio interface (EIAJ format)
  - Audio data serial interface for input and output
- Spindle motor servo
  - CLV digital servo
  - CAV digital servo
  - Switchable servo gain
- Audio circuits
  - Digital filter using 4-fold oversampling
  - Built-in D/A converter (1-bit D/A converter)
  - Built-in differential operational amplifier (secondary low pass filter)
- Operating voltage 4.75 to 5.25 V
- Other
  - Built-in playback pitch control function
  - Support for 12-fold speed playback (digital servo and signal processing blocks only)
  - Built-in support for jitter-free disc rotation synchronization playback
  - Power down mode that shuts off single-bit D/A converter, PCK output, and digital audio interface

■ Applications

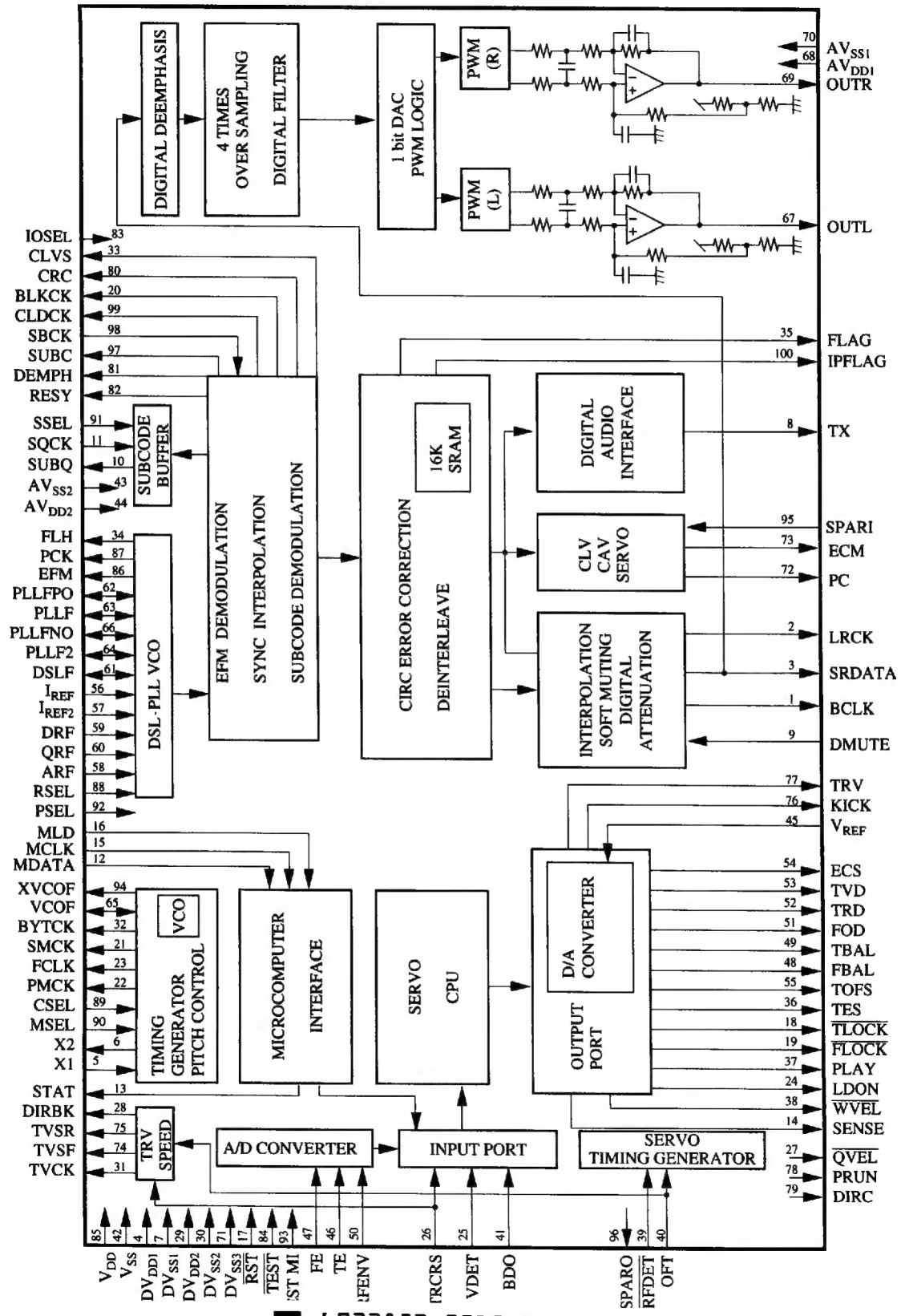
- CD–ROM drives

■ Pin Assignment



(TOP VIEW)
QFP100-P-1818B

■ Block Diagram



■ Pin Descriptions

Pin No.	Symbol	I/O	Function Description
1	BCLK	O	SRDATA bit clock output
2	LRCK	O	Left/right channel discrimination signal output "H" level: left channel audio data "L" level: right channel audio data
3	SRDATA	O	Serial data output
4	DV_{DD1}	I	Power supply for oscillator circuit
5	X1	I	Crystal oscillator circuit input pins (f = 16.9344 MHz, 33.8688 MHz)
6	X2	O	Crystal oscillator circuit output pins (f = 16.9344 MHz, 33.8688 MHz)
7	DV_{SS1}	I	Oscillator circuit ground
8	TX	O	Digital audio interface output signal
9	DMUTE	I	Muting input "H" level: muting
10	SUBQ	O	Subcode Q data output
11	SQCK	I	External clock input for subcode Q register
12	MDATA	I	Microcomputer command data input
13	STAT	O	Status signal (CRC, CLVS, TTSTOP, FCLV, SQOK, FLAG6, SENSE, $\overline{FLOCK}$, and $\overline{TLOCK}$)
14	SENSE	O	Sense signal output (OFT, FESL, NACEND, NAJEND, SFG, and NWTEND)
15	MCLK	I	Microcomputer command clock input (Data is latched at rising edge.)
16	MLD	I	Microcomputer command load signal input "L" level: load
17	$\overline{RST}$	I	Reset input "L" level: reset
18	$\overline{TLOCK}$	O	Tracking servo convergence signal "L" level: convergence
19	$\overline{FLOCK}$	O	Focus servo convergence signal "L" level: convergence
20	BLKCK	O	Subcode block clock signal (f_{BLKCK} = 75 Hz)
21	SMCK	O	If MSEL is "H" level, 8.4672 MHz clock signal output If MSEL is "L" level, 4.2336 MHz clock signal output
22	PMCK	O	88.2 kHz clock signal output
23	FCLK	O	Crystal frame clock signal output (f_{FCLK} = 7.35 kHz)
24	LDON	O	Laser ON signal output "H" level: ON
25	VDET	I	Vibration detection signal input "H" level: vibration detected
26	TRCRS	O	Track cross signal input
27	$\overline{QVEL}$	O	Quadruple-speed status signal output "L" level: quadruple-speed
28	DIRBK	O	Direction detection output for external track counter (Tristate output)
29	DV_{DD2}	I	Power supply for digital circuits
30	DV_{SS2}	I	Ground for digital circuits
31	TVCK	O	Pulse output for external track counter
32	BYTCK	O	When IOSEL is "H" level, byte clock signal output When IOSEL is "L" level, traverse stop signal output "H" level: stop mode
33	CLVS	O	Spindle servo phase synchronization signal output "H" level: CLV "L" level: rough servo
34	FLH	O	Speed detection result (Tristate output)
35	FLAG	O	Flag signal output
36	TES	O	Tracking error shunt signal "H" level: shunt
37	PLAY	O	Play signal output "H" level: play
38	$\overline{WVEL}$	O	Double-speed status signal output "L" level: double-speed

■ Pin Descriptions (continued)

Pin No.	Symbol	I/O	Function Description
39	$\overline{\text{RFDET}}$	I	RF detection signal input "L" level: detected
40	OFT	I	Offtrack signal input "H" level: offtrack
41	BDO	I	Dropout signal input "H" level: dropout
42	V_{SS}	I	Ground for digital circuits
43	AV_{SS2}	I	Ground for analog circuits (DSL, PLL, D/A converter output, and A/D converter)
44	AV_{DD2}	I	Power supply for analog circuits (DSL, PLL, D/A converter output, and A/D converter)
45	V_{REF}	I	Reference voltage for DA output (TVD, ECS, TRD, FOD, FBAL, TBAL, and TOFS)
46	TE	I	Tracking error signal input (analog input)
47	FE	I	Focus error signal input (analog input)
48	FBAL	O	Focus balance adjustment output
49	TBAL	O	Tracking balance adjustment output
50	RFENV	I	RF envelope signal input (analog input)
51	FOD	O	Focus drive output
52	TRD	O	Tracking drive output
53	TVD	O	Traverse drive output
54	ECS	O	Spindle motor drive signal (servo error signal output)
55	TOFS	O	Tracking offset adjustment output
56	I_{REF}	I	Reference current input pin
57	I_{REF2}	I	Reference current input pin (Connect to I_{REF} pin during 4-, 8-, and 12-speed operation.)
58	ARF	I	RF signal input
59	DRF	I	DSL circuit constant selection pins
60	QRF	I	DSL circuit constant selection pins
61	DSLF	I/O	DSL loop filter pin
62	PLFPO	I/O	PLLF charge pump output, "H" side
63	PLLF	I/O	PLL loop filter pin
64	PLLF2	I/O	PLL loop filter selection pin
65	VCOF	I/O	VCO loop filter pin
66	PLFNO	I/O	PLLF charge pump output, "L" side
67	OUTL	O	Left channel audio output
68	AV_{DD1}	I	Power supply for analog circuits (common use for left and right channel audio outputs.)
69	OUTR	O	Right channel audio output
70	AV_{SS1}	I	Ground for analog circuits (common use for left and right channel audio outputs.)
71	DV_{SS3}	I	Ground for digital circuits
72	PC	O	Spindle motor ON signal "L" level: ON (default)
73	ECM	O	Spindle motor drive signal (forced mode output) (tristate)
74	TVSF	O	Traverse speed control output for outward motion (tristate)
75	TVSR	O	Traverse speed control output for inward motion (tristate)
76	KICK	O	Kick pulse output (tristate)
77	TRV	O	Traverse forced feed output (tristate)

■ Pin Descriptions (continued)

Pin No.	Symbol	I/O	Function Description
78	PRUN	O	Pickup track crossing detection output
79	DIRC	O	Pickup track crossing direction detection output
80	CRC	O	Subcode CRC check result output "H" level: OK "L" level: no good
81	DEMPH	O	De-emphasis detection signal output "H" level: ON
82	RESY	O	When IOSEL is "H" level, RESY output, frame resynchronization signal "H" level: synchronize "L" level: out of sync. When IOSEL is "L" level, FLAG6 output, signal for resetting address for RAM used to de-interleave error correction data "L" level: address reset
83	IOSEL	I	Mode selection pin
84	$\overline{TEST}$	I	Test pin Keep this at "H" level
85	V_{DD}	I	Power supply for digital circuits
86	EFM	O	EFM signal output When IOSEL is "H" level, EFM signal output When IOSEL is "L" level, 16.9344-MHz clock output
87	PCK	O	PLL derived clock output with f_{PCK} = 4.3218 MHz (normal playback) DSL balance output (DSL correction output) during command input
88	RSEL	I	RF signal polarity selection pin "H" level: bright level is "H." "L" level: bright level is "L."
89	CSEL	I	Frequency specification pin for external crystal oscillator "H" level: 33.8688 MHz "L" level: 16.9344 MHz
90	MSEL/ LRCKIN	I	When IOSEL is "H" level, frequency selection pin for SMCK pin output "H" level: SMCK = 8.4672 MHz "L" level: SMCK = 16.9344 MHz When IOSEL is "L" level, LRCK input "H" level: left channel data "L" level: right channel data (SMCK output fixed at 16.9344 MHz)
91	SSEL/ BCLKIN	I	When IOSEL is "H" level, SUBQ pin output mode selection pin "H" level: buffered subcode Q mode. When IOSEL is "L" level, BCLK input "H" level: left channel data "L" level: right channel data (SUBQ pin output uses buffered subcode Q mode)
92	PSEL/ SRDATAIN	I	When IOSEL is "H" level, test pin Keep this at "L" level. When IOSEL is "L" level, SRDATA input
93	TESTMI	I	Test pin (pull-down pin) Keep this at "L" level.
94	XVCOF	I/O	VCO loop filter pin Keep this at "L" level when not used.
95	SPARI	I	FG signal input pin
96	SPARO	O	Test pin Leave this open. DSL balance output (DSL correction output) during command input
97	SUBC	O	Subcode serial output
98	SBCK	I	Serial clock input 2 for subcode serial output
99	$\overline{CLDCK}$	O	Subcode frame clock signal output pin. (f_{CLDCK} = 7.35 kHz)
100	IPFLAG	O	Interpolation flag signal output "H" level: interpolation

■ Package Dimensions (Unit: mm)

QFP100-P-1818B